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10/779,415	02/13/2004	Toshikazu Ogino	CU-3570 RJS	7772

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EXAMINER	
TIMORY, KABIR A	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/779,415	OGINO, TOSHIKAZU	
	Examiner	Art Unit	
	Kabir A. Timory	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on April 17, 2007. Claims 1 and 3 are amended. Claims 1-5 are pending in this application and have been considered below. Claims 6-8 are cancelled.

Response to Arguments

2. Applicant arguments filed on 4/20/2007 have been fully considered but they are not persuasive. The examiner's response to applicant's arguments is as follows:

Applicant's Argument: In page 5, applicant suggests that "the digital conversion part of the transmitter includes a comparator and a flip-flop circuit, the comparator having a non-inverting input and a grounded inverting input, and the digital conversion part performs the 1-bit quantization by inputting the modulated signal to the non-inverting input of the comparator, supplying an output of the comparator to the flip-flop circuit, and causing the flip-flop circuit to sample the output of the comparator at a rise time of a sampling clock, signal supplied thereto"

The Examiner's Response: Sutterlin et al. in figures 3, 5, and 8 clearly illustrates the digital conversion part having a comparator having high and low state of the signal and for further stability zero functioning is added, a flip-flop for sampling the signal, and 1-bit quantization.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hutchinson et al. (US Patent Number 5,812,607) in view of Sutterlin et al. (US Patent Number 5,471,209).

Regarding claim 1:

As shown in figure 1 Hutchinson et al discloses a communication system for transmitting a transmission signal in digital form (column 4, line 37) from a transmitter (column 1, line 56-57) to a receiver (column 1, line 62-63), wherein:

- the transmitter comprises: a modulation part modulating a carrier wave in accordance with the transmission signal according to frequency modulation (RF carrier is interpreted to be carrier wave) (column 4, lines 40-42); and
- a transmission part transmitting digital data into which the modulated signal is converted in the digital conversion part (this limitation is inherit because digital to analog converter DAC executes the conversion of the digital signal) (column 4, line 66-67 and column 5 line 1); and

- the receiver (column 1, line 62-63) comprises: a reception part receiving (column 5, line 34) the digital data transmitted from the transmission part (column 4, line 37); and
- a demodulation part (96 in figure 1) demodulating the digital data received by the reception part according to the frequency modulation (column 1, lines 65-76 and column 3, lines 1-4).

Hutchinson et al. discloses all of the subject matter as described above except for specifically teaching a digital conversion part performing l-bit quantization on a modulated signal obtained as a result of the modulation in the modulation part and Wherein the digital conversion part of the transmitter includes a comparator and a flip-flop circuit, the comparator having a non-inverting input and a grounded inverting input, and the digital conversion part performs the 1-bit quantization by inputting the modulated signal to the non-inverting input of the comparator, supplying an output of the comparator to the flip-flop circuit, and causing the flip-flop circuit to sample the output of the comparator at a rise time of a sampling clock, signal supplied thereto.

However, Sutterlin et al. in the same field of endeavor, teaches a digital conversion part performing l-bit quantization on a modulated signal obtained as a result of the modulation in the modulation part (305, 307 in figure 3); wherein the digital conversion part of the transmitter includes a comparator (811 in figure 8), and a flip-flop circuit (812 in figure 8), the comparator having a non-inverting input and a grounded inverting input (501 in figure 5), and the digital conversion part performs the 1-bit quantization by inputting the modulated signal to the non-inverting input of the

comparator, supplying an output of the comparator to the flip-flop circuit, and causing the flip-flop circuit to sample the output of the comparator at a rise time of a sampling clock, signal supplied thereto (column 8, lines 19-33).

One of ordinary skill in the art would have clearly recognized that in order to convert an analog signal to a digital signal, the signal needs to be transmitted in the samples form. Then each of these samples should be approximated or rounded off to the nearest quantized level and then coded as binary pulses. In order to perform the sampling and quantization process, a DAC (digital to analog converter) is needed. Moreover, for high-resolution sigma-delta A/D converter with architecture having an all-digital core and minimal analog components. It would be preferable if the comparator and loop filter of such architecture could be implemented using the digital logic cells of a gate array.

To increase the correlation between adjacent samples and have smaller prediction error in the system, it would have been obvious to one skill in the art at the time the invention was made to use 1-bit quantization technique as taught by Sutterlin et al. in sigma-delta converter having a digital logic gate core.

This technique uses only two levels for quantization and only one bit for error prediction. Also, it is advantageous to use 1-bit quantization technique because it does not produce the threshold inaccuracy noise, as would be the case with a multi-bit quantization. Moreover, 1-bit quantization is a very simple and inexpensive method of DAC conversion.

Regarding claim 3:

As shown in figure 1 Hutchinson et al discloses a communication device (transmitter is interpreted to be a device for transmission) (column 1, line 56-57) for transmitting a transmission signal in digital form (column 4, line 37), comprising:

- a modulation part modulating a carrier wave in accordance with the transmission signal according to frequency modulation (RF carrier is interpreted to be carrier wave) (column 4, lines 40-42);
- a digital conversion part (this limitation is inherit because digital to analog converter DAC executes the conversion of the digital signal) (column 4, line 66-67 and column 5 line 1); and
- a transmission part transmitting digital data into which the modulated signal is converted in the digital conversion part (column 4, line 66-67 and column 5 lines 1-4).

Hutchinson et al. discloses all of the subject matter as described above except for specifically teaching a digital conversion part performing l-bit quantization on a modulated signal obtained as a result of the modulation in the modulation part and the digital conversion part of the transmitter includes a comparator and a flip-flop circuit, the comparator having a non-inverting input and a grounded inverting input, and the digital conversion part performs the 1-bit quantization by inputting the modulated signal to the non-inverting input of the comparator, supplying an output of the comparator to the flip-flop circuit, and causing the flip-flop circuit to sample the output of the comparator at a rise time of a sampling clock, signal supplied thereto.

However, Sutterlin et al. in the same field of endeavor, teaches a digital conversion part performing l-bit quantization on a modulated signal obtained as a result of the modulation in the modulation part (305, 307 in figure 3); wherein the digital conversion part of the transmitter includes a comparator (811 in figure 8), and a flip-flop circuit (812 in figure 8), the comparator having a non-inverting input and a grounded inverting input (501 in figure 5), and the digital conversion part performs the 1-bit quantization by inputting the modulated signal to the non-inverting input of the comparator, supplying an output of the comparator to the flip-flop circuit, and causing the flip-flop circuit to sample the output of the comparator at a rise time of a sampling clock, signal supplied thereto (column 8, lines 19-33).

One of ordinary skill in the art would have clearly recognized that in order to convert an analog signal to a digital signal, the signal needs to be transmitted in the samples form. Then each of these samples should be approximated or rounded off to the nearest quantized level and then coded as binary pulses. In order to perform the sampling and quantization process, a DAC (digital to analog converter) is needed. Moreover, for high-resolution sigma-delta A/D converter with architecture having an all-digital core and minimal analog components. It would be preferable if the comparator and loop filter of such architecture could be implemented using the digital logic cells of a gate array.

To increase the correlation between adjacent samples and have smaller prediction error in the system, it would have been obvious to one skill in the art at the

time the invention was made to use 1-bit quantization technique as taught by Sutterlin et al. in sigma-delta converter having a digital logic gate core.

This technique uses only two levels for quantization and only one bit for error prediction. Also, it is advantageous to use 1-bit quantization technique because it does not produce the threshold inaccuracy noise, as would be the case with a multi-bit quantization. Moreover, 1-bit quantization is a very simple and inexpensive method of DAC conversion.

5. Claims 2, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hutchinson et al. and Sutterlin et al. as applied to claims 1 and 3 above, and further in view of Elberbaum et al. (US Patent Number 5,579,060).

Regarding claim 2:

As shown in (16 in figure 1) Hutchinson et al. discloses a communication system.

Hutchinson et al. and Sutterlin et al. disclose all of the subject matter as described above except for specifically teaching the transmitter further comprises an identification information insertion part inserting identification information into the transmission signal; and the receiver further comprises: an identification information extraction part extracting the inserted identification information from a demodulated

signal obtained as a result of the demodulation in the demodulation part; and an output control part enabling the demodulated signal to be output when the extracted identification information matches preset identification information, and disabling the demodulated signal from being output when the extracted identification information fails to match the preset identification information.

However, Elberbaum et al. in the same field of endeavor, teaches transmitter (26 in figure 1) further comprises

- an identification information insertion part inserting identification information into the transmission signal (column 3, lines 46-51); and
- the receiver (32 in figure 1) further comprises: an identification information extraction part extracting the inserted identification information (column 3, lines 51-57) from a demodulated signal obtained as a result of the demodulation in the demodulation part (column 13, lines 48-52); and
- an output control part (the control circuit is interpreted to be the output control part) (100 in figure 7) enabling the demodulated signal to be output when the extracted identification information (column 3, lines 46-51) matches preset identification information (predetermine value is interpreted to be the preset identification information) (column 8, lines 53-55), and
- disabling the demodulated signal from being output when the extracted identification information fails to match the preset identification information (column 11, lines 12-15).

One of ordinary skill in the art would have clearly recognized that in a communication system in order to identify signals transmitted from a transmitter to receiver system, an identification code comparing circuit for generating the identification code is needed. The receiver includes an identification circuit, which may further include a memory for storing identification data such as predetermined signal information. Moreover, an extracting circuit is needed for extracting the identification code signal and to generate the predetermined identification code signal and an output control circuit for retrieving the identification data from the memory and feeding the extracted signal only when the identification code signal corresponds to the identification code allotted to it.

To increase the probability of receiving error free signal, it would have been obvious to one skill in the art at the time the invention was made to include an identification code circuit which, further includes a memory for storing predetermined identification data, an output control circuit, and a comparator circuit in the receiver as taught by Elberbaum et al. to identify any mismatch signal in the system.

Advantageously, the identification code circuit with predetermined identification code signal, an output control circuit, and comparator circuit provide means for verification of the generated signals and basis for error free transmission.

Regarding claim 4:

As shown in (16 in figure 1) Hutchinson et al. discloses a communication device.

Hutchinson et al. and Sutterlin et al. disclose all of the subject matter as described above except for specifically teaching an identification information insertion part inserting identification information into the transmission signal.

However, Elberbaum et al. in the same field of endeavor, teaches an identification information insertion part inserting identification information into the transmission signal (code injection circuit is interpreted to be insertion part) (74 in figure 4, column 10, lines 6-9).

One of ordinary skill in the art would have clearly recognized that in a communication system in order to inject the identification information into a transmission line an identification insertion circuit is needed. Also, the system further includes an identification circuit and identification code comparing circuit for generating the identification code. The identification circuit may further include a memory for storing identification data such as predetermined signal information. This predetermined signal information is used to compare the output signals. In doing so, the comparing circuit identifies any mismatch signal is the system. Moreover, a control circuit is needed for extracting the signal from transmission line when the signal identification coded matches the signal predetermined data.

To increase the probability of receiving error free signal, it would have been obvious to one skill in the art at the time the invention was made to include an identification insertion circuit, an identification code circuit and a comparator circuit in the transmission as taught by Elberbaum et al. to identify any mismatch signal in the system.

Advantageously, the identification code circuit with predetermined identification code signal, an output control circuit, and comparator circuit provide means for verification of the generated signals and basis for error free transmission.

Regarding claim 5:

As shown in (16 in figure 1) Hutchinson et al. discloses a communication device as claimed in claim 4, wherein the transmitted digital data (column 4, line 37) is received by a receiver (column 1, line 62-63).

Hutchinson et al. and Sutterlin et al. disclose all of the subject matter as described above except for specifically teaching the identification information is preset in the receiver.

However, Elberbaum et al. in the same field of endeavor, teaches the identification information is preset in the receiver (predetermine value is interpreted to be the preset identification information) (column 8, lines 53-55).

One of ordinary skill in the art would have clearly recognized that in a communication system in order to identify signals transmitted from a transmitter to receiver system, an identification code comparing circuit for generating the identification code is needed. The receiver includes an identification circuit, which may further include a memory for storing identification data such as predetermined signal information. Moreover, an extracting circuit is needed for extracting the identification code signal and to generate the predetermined identification code signal and an output controller circuit for retrieving the identification data from the memory. In doing so, the processed signal can be identified by the identification code signal means. This

predetermined signal information is used to compare the output signals. In doing so, the comparing circuit identifies any mismatch signal is the system.

To increase the probability of receiving error free signal, it would have been obvious to one skill in the art at the time the invention was made to include an identification code circuit which, further includes a memory for storing predetermined identification data, and a comparator circuit in the receiver as taught by Elberbaum et al. to identify any mismatch signal in the system.

Advantageously, the identification code circuit with predetermined identification code signal, an output control circuit, and comparator circuit provide means for verification of the generated signals and basis for error free transmission.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kabir A. Timory whose telephone number is 571-270-1674. The examiner can normally be reached on 6:30 AM - 3:00 PM Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kabir A. Timory
July 5, 2007

SHUWANG LIU
SUPERVISORY PATENT EXAMINER